What is claimed is:

1. A method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, comprising the steps of:

depositing on the gate dielectric polysilicon crystals of substantially a first size; and

contiguously with the crystals of the first size depositing directly thereon additional polysilicon crystals of substantially a second size.

2. The method according to claim 1, wherein:

the first crystal size is larger than the second crystal size.

3. The method according to claim 1, wherein:

the first crystal size is smaller than the second crystal size.

4. A method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, comprising the step of:

controlling a variation of at least one of temperature, pressure, and flow rate of a continuous flow of silane or related silicon precursor species while depositing polysilicon therefrom as crystals of correspondingly controlled grain size.

5. The method according to claim 4, wherein:

the variation is controlled in step-wise manner, to thereby form a multi-region polycrystalline silicon deposit comprising regions having crystals of respective grain sizes.

6. The method according to claim 5, wherein:

crystals deposited in a first region adjacent to the gate dielectric have a first grain size selected to maximize dopant activation near the gate dielectric and a second region that has crystals of a second grain size deposited more distantly from the gate dielectric.

7. A method of forming a polycrystalline silicon structure in which crystal grain size varies as a function of depth, comprising the step of:

controlling a variation of at least one of temperature, pressure, and flow rate of a silane gas while depositing silicon therefrom, to thereby control the crystal grain size as a function of depth in the deposited polysilicon structure.

8. The method according to claim 7, wherein:

the polysilicon structure comprises a plurality of regions having respective grain sizes.

9. The method according to claim 8, wherein:

the polycrystalline silicon structure is a gate electrode formed on a gate dielectric, and comprises a first region having a first crystal grain size and a second region formed thereon and having a second grain size,

wherein the first and second grain sizes are selected to maximize dopant activation in the first region and to achieve a specific resistance in the second region.

10. The method according to claim 9, further comprising:

a third region formed on the second region and having crystals of a third grain size, to further tailor the resistance of the gate conductor structure.

11. The method according to claim 8, wherein:

the electrical resistance of the deposited silicon varies inversely with the controlled pressure.

12. The method according to claim 7, comprising the further step of:

providing a controlled flow of a dopant gas during a selected portion of the step of depositing polysilicon, to thereby enable selected doping or counter-doping of a portion of the deposited polysilicon.

13. The method according to claim 12, wherein:

the dopant gas is selected to provide one of a p-type or an n-type doping during a final portion of the step of depositing polysilicon.

14. The method according to claim 7, comprising the further step of:
forming a layer rich in carbon atoms at a selected stage of the silicon deposition.

15. The method according to claim 7, comprising the further step of:
forming a layer of silicon-germanium at a selected stage of the silicon deposition.

16. The method according to claim 7, wherein:
the variation is controlled to deposit the polysilicon so that the crystal grain size varies monotonically during the deposition of the polysilicon.

17. A CMOS transistor comprising a gate conductor formed on a gate dielectric, wherein the gate conductor comprises a multi-region polycrystalline silicon, comprising:
a first region adjacent the dielectric and comprising silicon crystals of a first grain size; and
a second region formed contiguously with and over the first region and comprising silicon crystals of a second grain size.

18. The CMOS transistor according to claim 17, wherein:
the first and second grain sizes are selected to maximize a dopant activation near the gate dielectric in the first region and to achieve a specific resistance in the second region.

19. The CMOS transistor according to claim 18, wherein:
an upper portion of the polysilicon structure is consumed by silicide.

20. The CMOS transistor according to claim 18, further comprising:
a third region formed contiguously with and over the second region, the third region serving to further tailor the resistance of the gate conductor.

21. A doped polysilicon resistor structure, comprising:
an insulator; and

a multi-region polycrystalline silicon conductor structure, comprising regions having silicon crystals of respectively different sizes, formed over the insulator.

22. The structure according to claim 20, wherein:
the silicide formation is blocked by a layer of nitride.